Remarks/Arguments

Claim Summary

By this Amendemnt, claims 1-2 and 11-15 have been canceled, new claims 16 and 17 have been added, and claims 3 and 4 have been revised.

Accordingly, claims 3-10 and 16-17 are now pending in the application, where claims 5-10 have been withdrawn from consideration.

35 U.S.C. ¶103

Claims 1-4, 11, 14 and 15 stand rejected under 35 U.S.C. ¶103 as being unpatentable over the admitted prior art (APA) in view of Masakuni et al. (JP 10-284678) and Shimizu et al. (US 6211576). Claims 12 and 13 were rejected under 35 U.S.C. ¶103 as being unpatentable over the APA in view of Masakuni et al., Shimizu et al., Stearns et al. (US 5895967) and Kirkman (US 6064113).

Reconsideration of the rejections under 35 U.S.C. ¶103 is requested with respect to the non-pending claims 3-4 and 16-17.

As Applicants understand the rejections, the Examiner apparently contends that one of ordinary skill in the art would be motivated to (a) adopt the common wirings 5c (FIG. 2) of Masakuni et al. in the APA (FIGS. 1 and 2), and (b) once adopted, replace the common wirings 5c (FIG. 2) of Masakuni et al. with a planar structure such as those illustrated in Shimizu et al. Applicants disagree on both counts.

That is, Applicants contend that one of ordinary skill would not be motivated to modify the APA in view of Masakuni et al. in the manner suggested by the Examiner. That is, in Masakuni et al., only a subset of the outermost balls 6 are for power or ground connection. Accordingly, the balls 6 of Masakuni et al. do not rest directly on the common wiring 5c, and instead the common wiring 5c is offset to the outer portion of the TCP relative to the balls 6. The APA, however, includes both power and ground ball electrodes on

both sides of the substrate surface (FIG. 2), and it would not be obvious to add additional common wirings which are offset from the ball electrodes in the manner shown by Masakuni et al.

Further, Shimuzu et al. is directed to a wafer-level package in which signal lines are formed by wafer-level patterning of conductive layers to form connections between pads and solder bump mounts. In contrast, the presently claimed invention is directed to a package in which a substrate is mounted to a semiconductor chip, and in which it is necessary to form wirings (such as bonding wires or lead wires) between an upper surface of the substrate and pads of the semiconductor chip. One of ordinary skill in the art would not apply the wafer-level package techniques of Shimuzu et al. to a package such as that of the present claims.

Morever, as pointed out in a previous response, Masakuni et al. is directed to a tape carrier package (TCP) in which the bump electrodes and outer leads are formed in or on a flexible tape, such as polyimide. One of ordinary skill would not be motivated to embed a ground plane or power plane electrode in a TCP in which flexibility of the carrier is desired.

Even assuming *arguendo* that one of ordinary skill would to look to the Shimizu et al. reference as suggest by the Examiner, such a person would undoubtedly look to the arrangement such as that illustrated in FIG. 8 of Shimizu et al. However, the ground and power plates of Shimizu et al. are not located on opposite sides only of a central region as recited in now-pending claim 16. In fact, Shimizu et al. clearly teaches away from such an arrangement. Col. 10, lines 19-24.

For at least these reasons and the reasons already of record, Applicants content that claims 3-4 and 26-18 define over the prior art.

Conclusion

No other issues remaining, reconsideration and favorable action upon the elected Claims 3-4 and 16-18 now-pending in the application are requested.

Respectfully submitted,

KI-WHAN SONG

By: 

Adam C. Volentine
Reg. No. 33,289

August 15, 2005

VOLENTINE FRANCOS, PLLC
12200 Sunrise Valley Drive, Suite 150
Reston, VA 20191
(703) 715-0870